REMARKS

The claims are claims 1 to 15.

The application has been r amended at many locations to correct minor errors and to present uniform language throughout. These amendments renumber the tables from Table 1 rather than the previous Table 4. These amendments include an update of the status of the copending patent applications cited on pages 9, 23 and 27.

Claims 1, 2 and 6 to 13 were rejected under 35 U.S.C. 102(e) as anticipated by Peleg et al U.S. Patent No. 5,983,256.

Claim 1 recites subject matter not anticipated by Peleg et al. Claim 1 recites "rounding the combined product to form an intermediate result." The OFFICE ACTION cites Peleg et al at column 15, lines 20 to 25, column 12, lines 64 to 68 and column 14, lines 36 to 42 and Table 6a with relation to claim 1. None of these portions of Peleg et al include any teaching on rounding. Peleg et al states at column 15, lines 20 to 25:

> "The disclosed multiply-add instruction can be used to multiply two complex numbers in a single instruction as shown in Table 6a. As previously described, the multiplication of two complex number (e.g., r_1 i_1 and r_2 i_2) is performed according to the following equation:"

This text fails to mention rounding. Peleg et al states at column 12, lines 64 to column 13, line 2 (including the portion cited in the OFFICE ACTION):

> "In one embodiment of the invention, the multiply-add and multiply-subtract instructions operate on signed packed data and truncate the results to avoid any overflows. In addition, these instructions operate on packed word data and the Result is a packed double word. However, alternative embodiments could support these instructions for other packed data types."

This text fails to mention rounding. Peleg et al states at column 14, lines 36 to 42:

> "This wastes data lines and circuitry that are used for the bits that are higher than bit sixteen for Source1 and Source2, and higher than bit thirty two for the Result. As well, the entire 64-bit result generated by the prior art processor may not be of use to the programmer. Therefore, the programmer would have to truncate each result."

This text fails to mention rounding. Likewise Table 6a on column 15 of Peleg et al includes no mention of rounding. Thus no portion of Peleg et al cited regarding claim 1 teaches rounding. In the absence of any citation to the teaching of rounding in the reference, claim 1 is allowable over Peleg et al.

Claim 6 recites subject matter not anticipated by Peleg et al. Claim 6 recites "when an overflow occurs, the intermediate result will wrap from a largest positive value to a smallest negative value." Peleg et al states at column 12, lines 64 to 68 (cited in the OFFICE ACTION):

> "In one embodiment of the invention, the multiply-add and multiply-subtract instructions operate on signed packed data and truncate the results to avoid any overflows."

This portion of Peleg et al teaches truncation to avoid overflows. This teaching fails to state any action "when an overflow occurs" as recited in claim 6. This portion of Peleg et al fails mention a "wrap from a largest positive value to a smallest negative value'" as recited in claim 6. Accordingly, claim 6 is allowable over Peleg et al.

Claim 7 recites subject matter not anticipated by Peleg et al. Claim 7 recites "an overflow is not reported when an overflow occurs." The cited portion of Peleg et al quoted above teaches truncation to avoid an overflow. This portion of Peleg et al

includes no teaching of any action taken "when an overflow occurs." The teaching of avoiding an overflow cannot make obvious the claimed action taken upon an overflow. Accordingly, claim 7 is allowable over Peleg et al.

Claim 9 recites subject matter not anticipated by Peleg et al. Claim 9 recites "the step of forming treats a one of the first pair of elements as a signed number value and treats another one of the first pair of elements as an unsigned number value." The OFFICE ACTION cites Table 6a of column 15 of Peleg et al as anticipating this subject matter. Peleg et al does disclose signed and unsigned packed integer formats at column 1, line 28 to column 11, line 2 and illustrates these formats at Figures 5a, 5b and 5c. However, the portion of column 15 of Peleg et al cited by the Examiner fails to state that the complex number multiplication instruction treats one operand as a signed integer and one as an unsigned integer as recited in claim 9. On the contrary, Peleg et al states at column 11, lines 52 to 55:

> "Control bit S 612, bit ten, indicates the use of a signed operation. If S 612 equals one, then a signed operation is performed. If S 612 equals zero, then an unsigned operation is performed."

The use of a single bit in the instruction coding to set a signed or an unsigned operation implies that the operands are treated either both as signed integers or both as unsigned integers. The instruction coding of Figure 6a of Peleg et al does not have the capability of treating one operand as signed and the other as unsigned. Accordingly, claim 9 is allowable over Peleg et al.

Claim 13 recites subject matter not anticipated by Peleg et al. Claim 13 recites "an arithmetic circuit connected to receive a plurality of products from the plurality of multipliers, the arithmetic circuit having a provision for mid-position rounding

responsive to the rounding dot product instruction." The Applicant respectfully submits that Peleg et al fails to disclose any rounding. The only structures disclosed in Peleg et al that could embody the claimed arithmetic circuit are adder/subtractors 850 and 851 illustrated in Figure 8. These adder/subtractors do not include "a provision for mid-position rounding responsive to the rounding dot product instruction" as recited in claim 13. Accordingly, claim 13 is allowable over Peleg et al.

Claims 3 to 5 and 14 were rejected under 35 U.S.C. 103 (a) as made obvious by the combination of Peleg et al. U.S. Patent No. 5,983,256 and Suzuki et al. U.S Patent No. 5,276,634.

Claim 3 recites subject matter not made obvious by the combination of Peleg et al and Suzuki et al. Claim 3 recites "the step of rounding adds a rounding value to the combined product via an arithmetic circuit having a first input receiving said first product, a second input receiving said second product and a carry input to a mid-position receiving said rounding value to form the intermediate result." As taught in the application at page 25, lines 3 to 10, the recited mid-position refers to a middle bit position in the arithmetic circuit. Suzuki et al includes no such disclosure. Figure 25 of Suzuki et al illustrate only two inputs to product generate adder 265 and to mantissa adder 269. Further, Suzuki et al fails to teach any mid-position input as claimed. Accordingly, claim 3 is allowable over the combination of Peleg et al and Suzuki et al.

Claim 14 recites subject matter not made obvious by the combination of Peleg et al and Suzuki et al. Claim 14 recites "the arithmetic circuit has a carry input connected to a mid-position, wherein the carry input is asserted in response to the rounding dot product instruction." The Applicant respectfully submits that Suzuki et al fails to teach or make obvious a carry input at a mid-position. Figure 24 of Suzuki et al illustrate the output from

round value generator 267 supplied to one input of mantissa adder 269 as selected by selector 268. Because selector 268 may alternatively select the output of product generate adder 265, this is an ordinary input to mantissa adder 269 and not the mid-position carry input claimed. Accordingly, claim 14 is allowable over the combination of Peleg et al and Suzuki et al.

The Applicant respectfully submits that all the present claims are allowable for the reasons set forth above. Therefore early reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address to facilitate prosecution.

Texas Instruments Incorporated
P.O. Box 655474 M/S 3999
Dallas, Texas 75265
(972) 917-5290
Fax: (972) 917-4418

Respectfully submitted,

Robert D. Marshall, Jr.
Reg. No. 28,527